FIG. 1

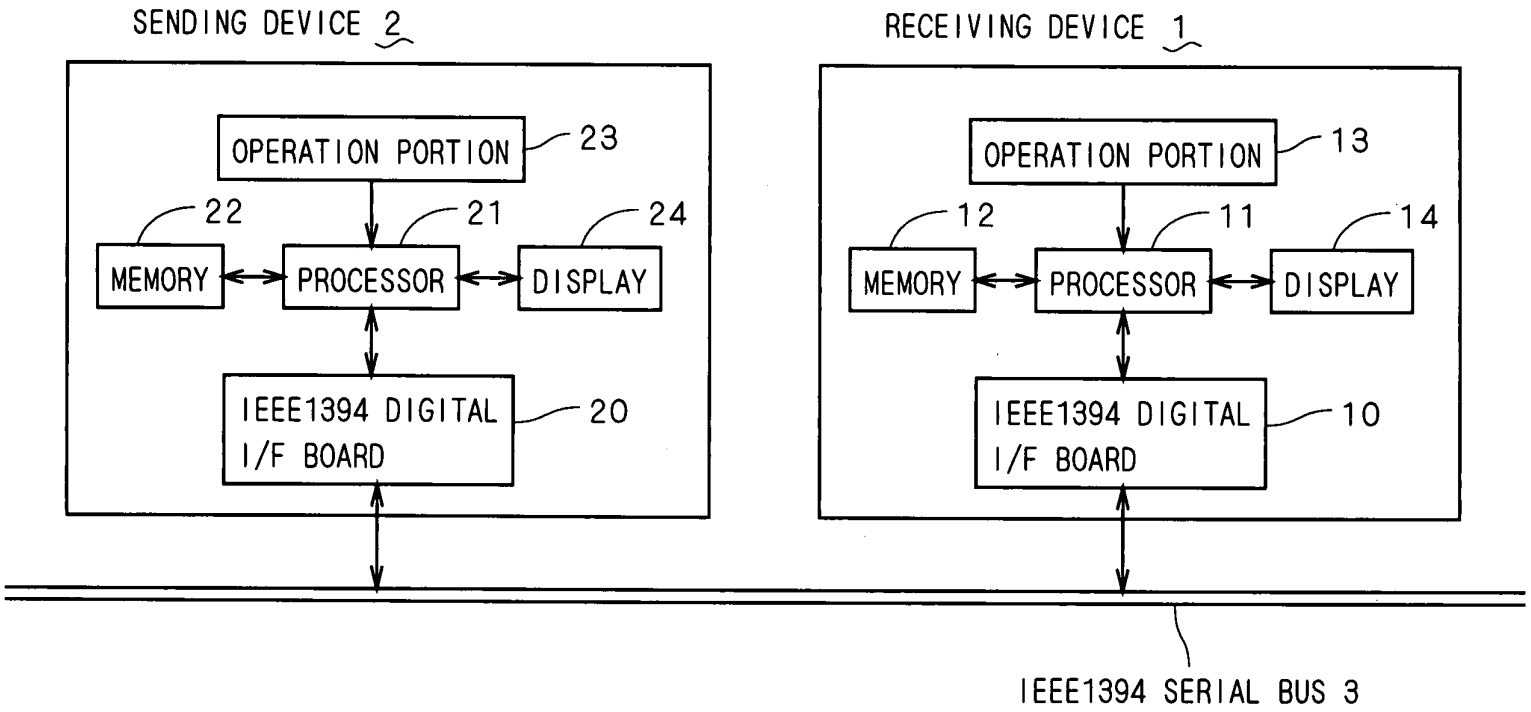
SENDING DEVICE 2
OPERATION PORTION
23
22
21
24
MEMORY
PROCESSOR
DISPLAY
IEEE1394 DIGITAL I/F BOARD
20
RECEIVING DEVICE 1
OPERATION PORTION
13
12
11
14
MEMORY
PROCESSOR
DISPLAY
IEEE1394 DIGITAL I/F BOARD
10
IEEE1394 SERIAL BUS 3

FIG. 2

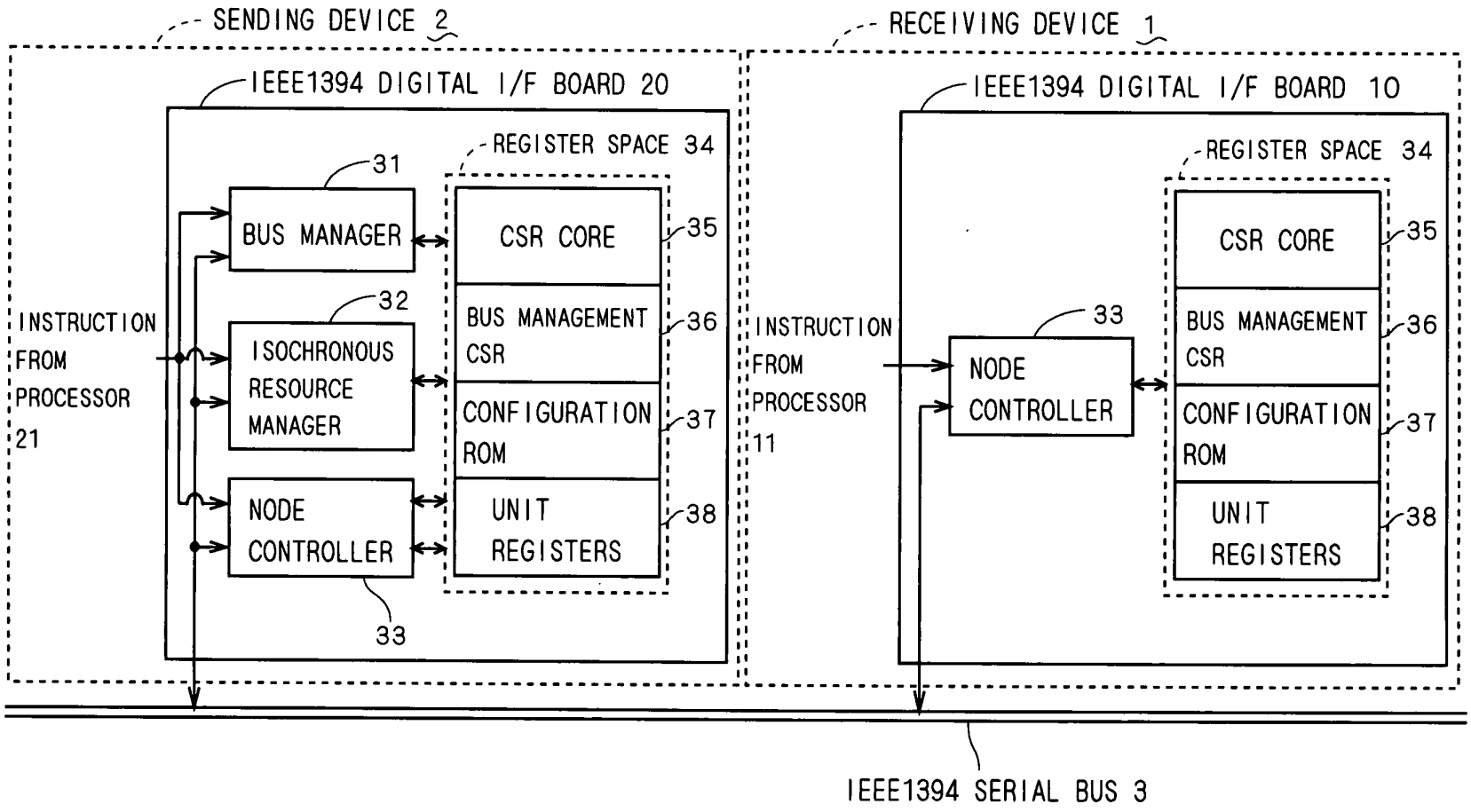
SENDING DEVICE 2
RECEIVING DEVICE 1
IEEE1394 DIGITAL I/F BOARD 20
IEEE1394 DIGITAL I/F BOARD 10
REGISTER SPACE 34
REGISTER SPACE 34
31
BUS MANAGER
32
ISOCHRONOUS RESOURCE MANAGER
NODE CONTROLLER
33
CSR CORE
35
BUS MANAGEMENT CSR
36
CONFIGURATION ROM
37
UNIT REGISTERS
38
INSTRUCTION FROM PROCESSOR 21
INSTRUCTION FROM PROCESSOR 11
33
NODE CONTROLLER
CSR CORE
35
BUS MANAGEMENT CSR
36
CONFIGURATION ROM
37
UNIT REGISTERS
38
IEEE1394 SERIAL BUS 3

FIG. 3

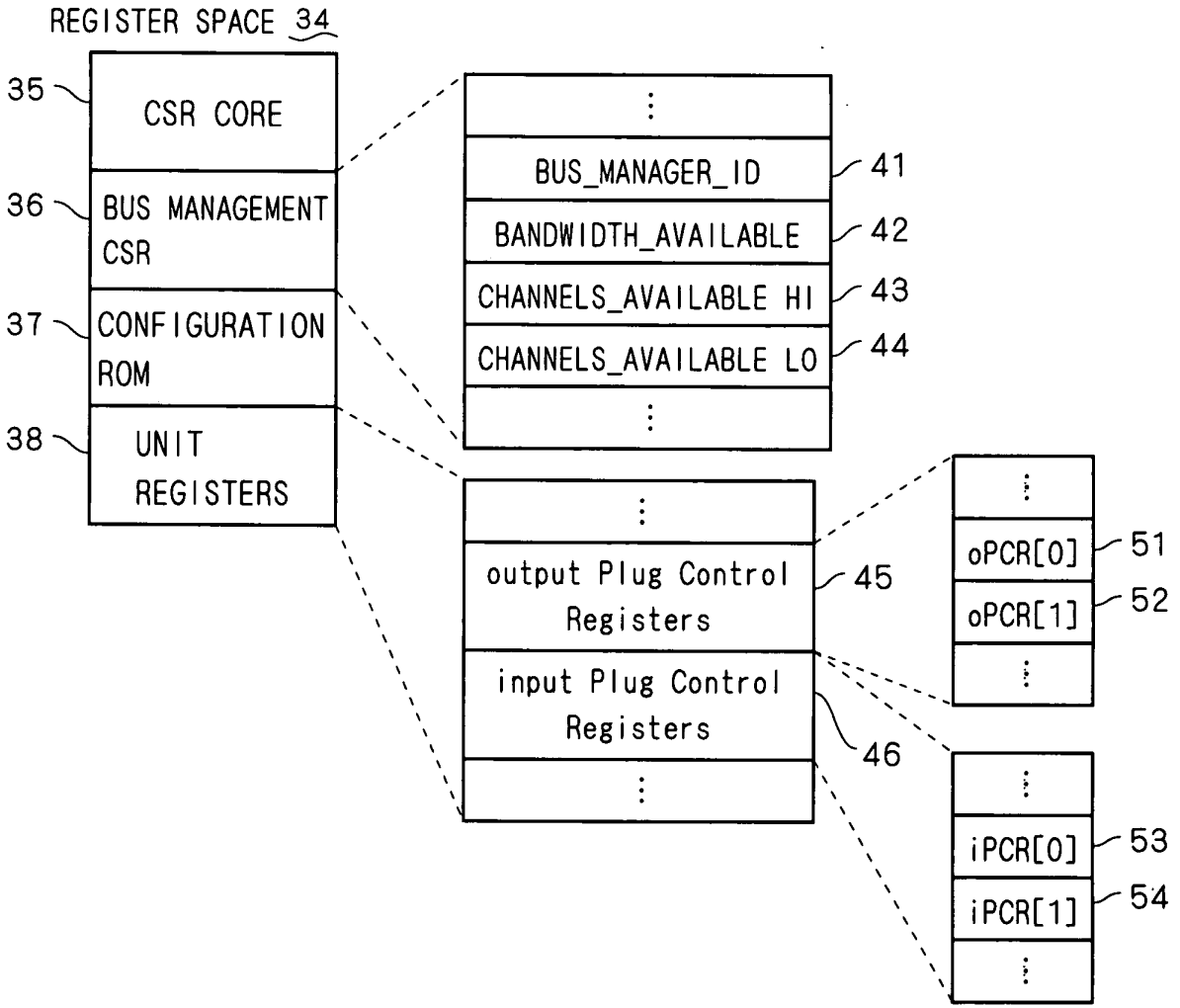
REGISTER SPACE 34
35
CSR CORE
36
BUS MANAGEMENT CSR
37
CONFIGURATION ROM
38
UNIT REGISTERS
BUS_MANAGER_ID
41
BANDWIDTH_AVAILABLE
42
CHANNELS_AVAILABLE HI
43
CHANNELS_AVAILABLE LO
44
output Plug Control Registers
45
input Plug Control Registers
46
oPCR[0]
51
oPCR[1]
52
iPCR[0]
53
iPCR[1]
54

FIG. 4

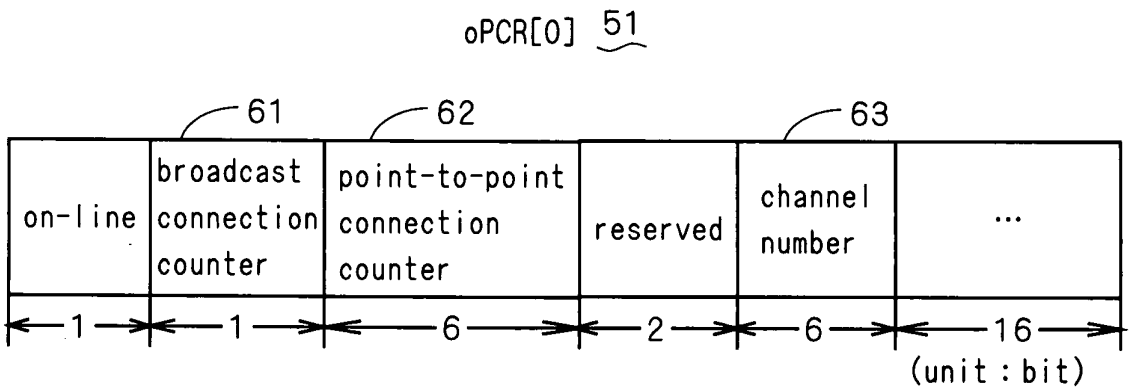
oPCR[0] 51
61
62
63
on-line
broadcast connection counter
point-to-point connection counter
reserved
channel number
...
1
1
6
2
6
16
(unit : bit)

FIG. 5

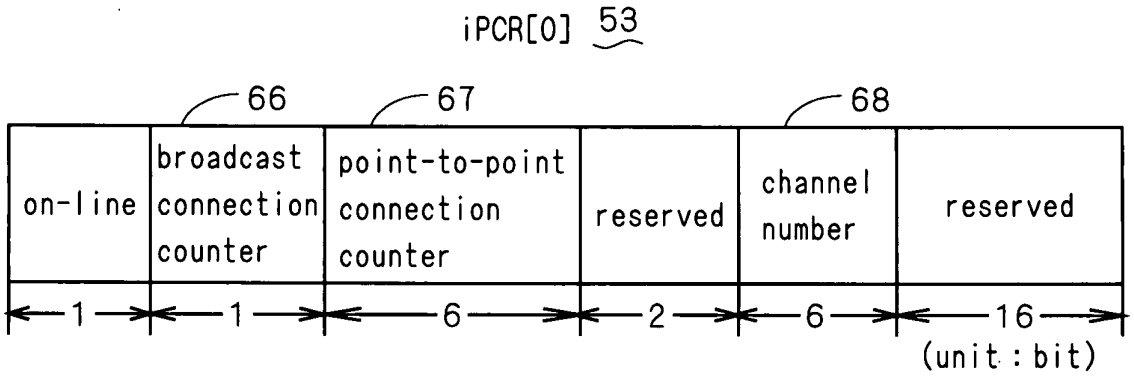
iPCR[0] 53
66
67
68
on-line
broadcast connection counter
point-to-point connection counter
reserved
channel number
reserved
1
1
6
2
6
16
(unit : bit)

FIG. 6

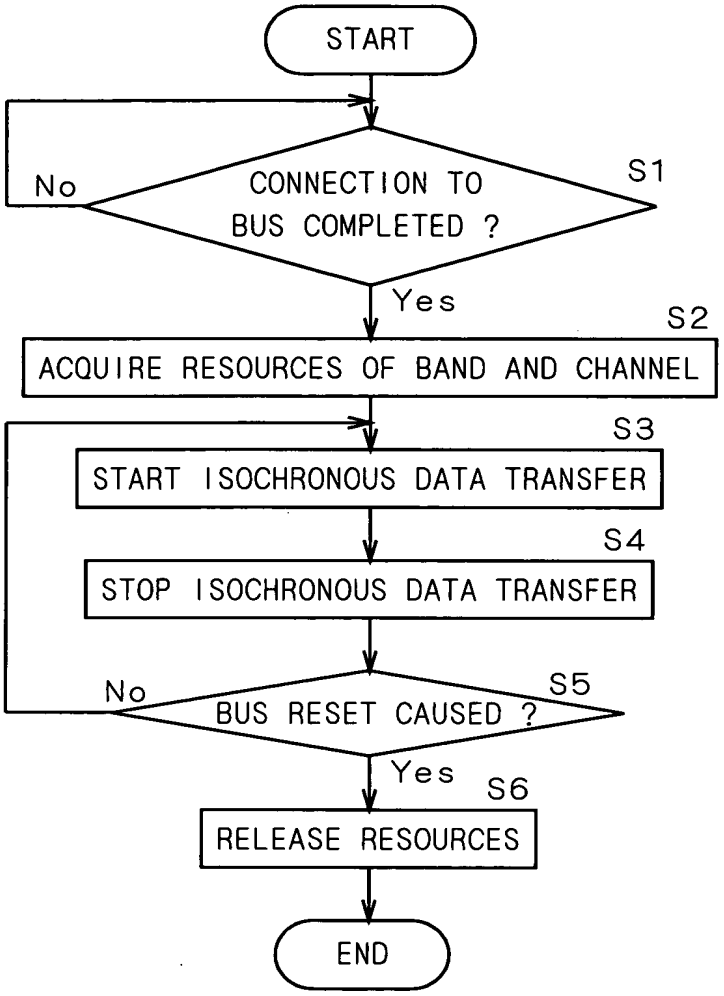
START
CONNECTION TO BUS COMPLETED ?
S1
No
Yes
S2
ACQUIRE RESOURCES OF BAND AND CHANNEL
S3
START ISOCHRONOUS DATA TRANSFER
S4
STOP ISOCHRONOUS DATA TRANSFER
BUS RESET CAUSED ?
S5
No
Yes
S6
RELEASE RESOURCES
END

FIG. 7 PRIOR ART

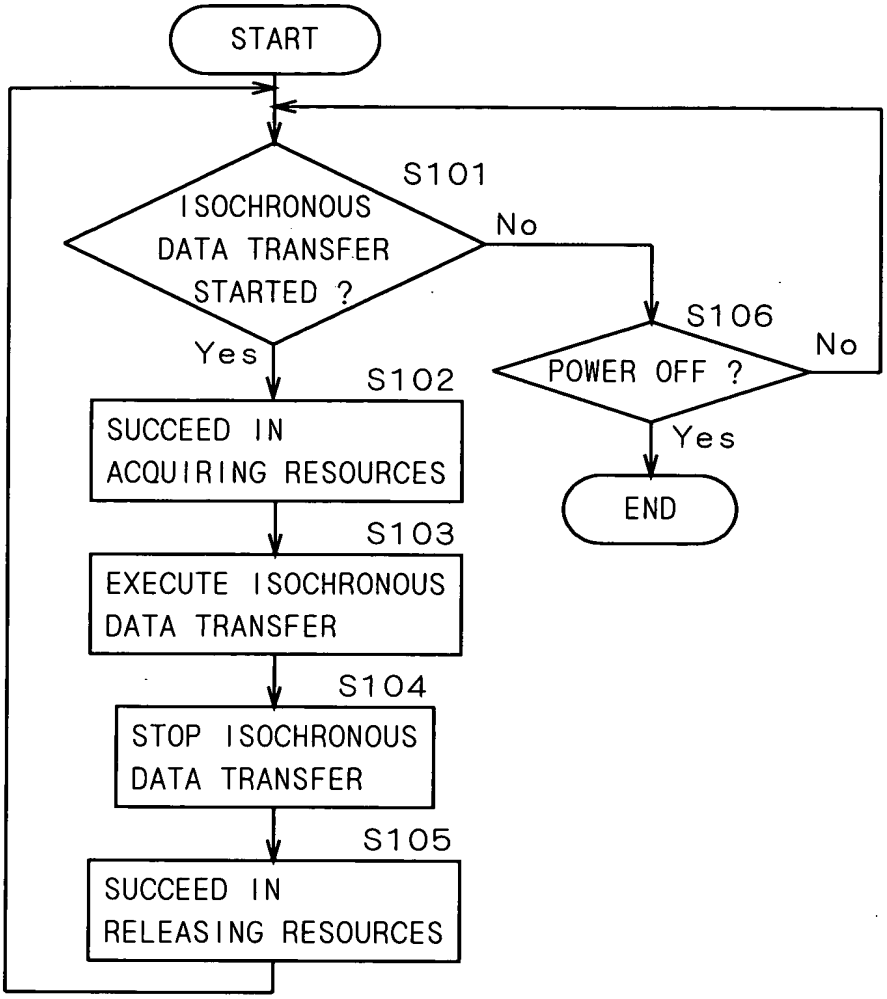
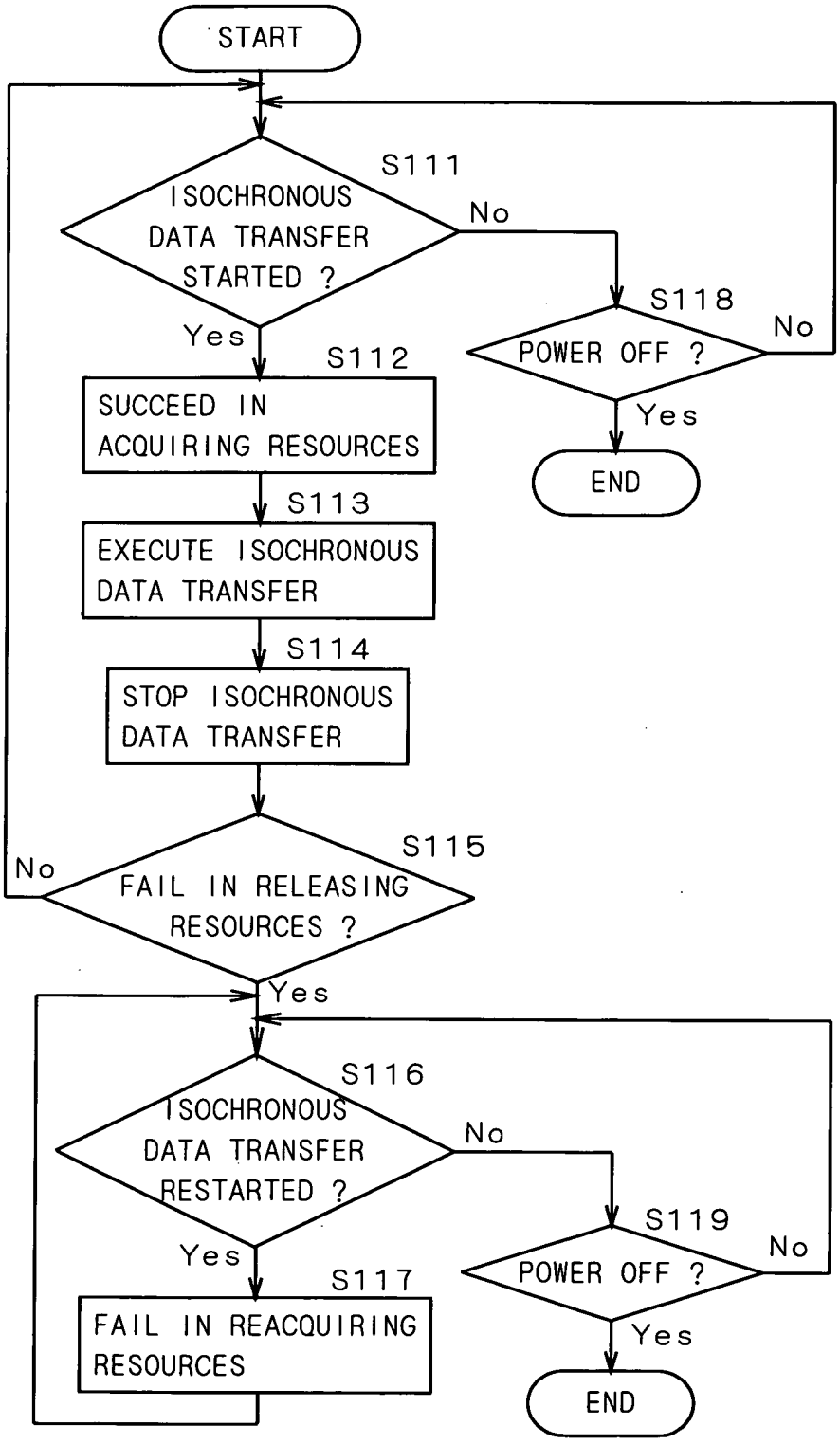
FIG. 8 PRIOR ART